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Designing of Low Power CNTFET Based D Flip-Flop Using Forced Stack Technique

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ABSTRACT
Low Power devices in small packages is the need of present and future electronic devices. Electronics Industry is making devices which can be planted in human bodies. CMOS Technology won't be able to deliver such devices because it shows short channel effects in Nano scale. So, to overcome the problems of CMOS technology we use CNTs (Carbon Nano Tubes). In electronic devices, power is consumed by various elements like flip-flop, latches, clock sources. So in order to reduce power of a system we used to reduce power consumed by flip-flops.
In this paper we design an existing flip-flop "Low power clocked pass transistor flip-flop (LCPTFF)" on CNTFET using Stanford CNTFET model for reference. We propose a design of CNTFET based Forced Stack Low Power Clocked Pass Transistor Flip-Flop (CN-FS-LCPTFF) and observe 12% to 25% power reduction in various conditions like temperature change, CNTFET diameter change, and different voltage supply.
Keywords **–** CNTFET, CN-LCPTFF, CN-FS-LCPTFF, SWCNT, CMOS

I. INTRODUCTION

VLSI Industry is witnessing rapid change of technology in past few years. As the CMOS channel is continuously scaling down into nanoscale region for concern of low power ,small area and high speed. While scaling makes the channel shorter or narrower, which introducing the short channel and narrow channel effects, changes the device parameter dramatically due to which unnecessary power consumption comes into the picture[1]. All these effects degrade the performance of the circuit functionality and that is why during last few years' researchers' have shown their interest in nanotechnology and nanoelectronics. This research leads us to Carbon Nanotubes(CNTs) because of its superior electrical , thermal and mechanical properties[2]. Carbon nanotubes Field Effect transistor(CNTFET) is the best alternate of traditional Silicon technology because the operation principle and structure of device is quite similar to CMOS devices, so we can use the old CMOS design and fabrication too[3]. CNTFET also has good current carrying ability.

Our main focus in this paper is reducing the power consumption and we will use every possible way to reduce it in our circuit without changing its functionality, as power consumption is the fundamental problem. In the recent era of VLSI design so many researcher's have focused on the power consumption however there is no universal way to avoid tradeoffs between power, delay and area.[4] So designer has to choose the best technique which satisfies the requirements of application and product.

Power consumption in the CNTFET consists of dynamic and static component as in CMOS circuits. Dynamic power dissipation is due to the switching of transistors and static power consumed regardless of transistor switching. On 180nm and above technology, 90% of power consumption is dynamic but the feature size of the devices shrinks, e.g. 65 nm , the sub-threshold leakage power dissipation of a chip may equivalent to dynamic power dissipation[5].

II. CNTFET

CNTs are formed by rolling the sheets of graphene at specific and discrete angle known as chiral angle as shown in the Fig. 1. CNT was first developed by Sumio Iijima of NEC in 1991[6].

The single walled CNT (SWCNT) can be metallic or semiconducting depends on its chirality vector (m , n)[7] which is an angle and direction in which the sheet is rolled. CNT will be metallic if m=n or (m-n=3i) where 'i' is an integer otherwise the CNT is considered as a Semiconductor. One of the most important parameter of CNTs is its diameter which is predefined during the generation process and is denoted by D_{cnt} [7]:

$$D_{cnt} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (1)$$

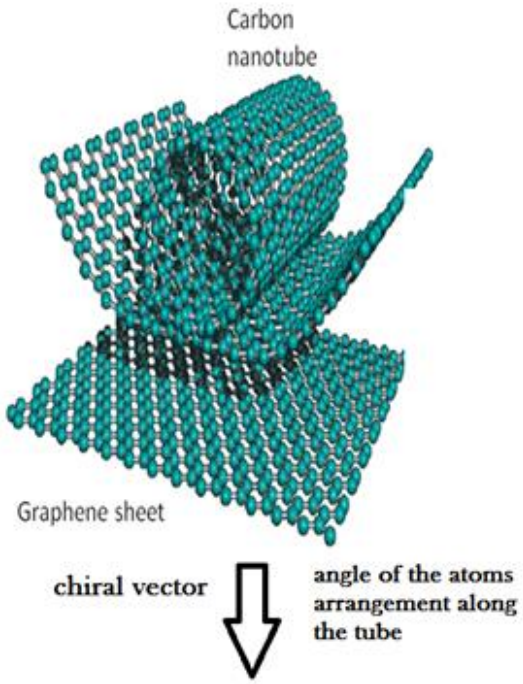

Fig.1: Carbon Nanotube Structure and Chiral Vector

Where a_0 = 0.142nm is the interatomic distance of carbon to carbon atom and its neighbor

CNTFET uses the semiconducting CNT which is utilized as a conducting channel between source and drain contacts under the gate terminal as shown in Fig.2.[8] The working of a CNTFET is similar to traditional MOSFET device but the manufacturing process is easier than that of MOSFET. The conductivity of the channel is controlled by

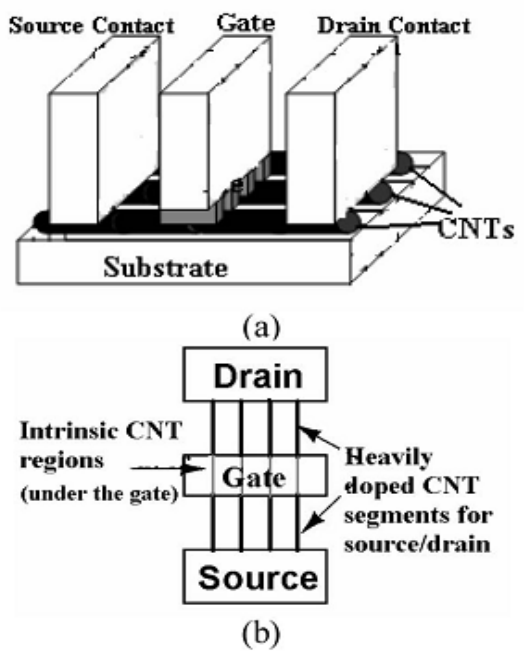

Fig. 1: Schematic Diagram of a CNTFET. (a) Cross Sectional View[8]

The gate which is quite similar to the MOSFET device but the capabilities of carrying current is better and this current is directly depeing on the number of tubes which affect the circuit speed directly. The threshold voltage of CNTFET which is an important factor is given as[8]:

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{cnt}}$$

Where, a=2.49A^o is carbon-carbon atom distance, V_π = 3.033eV is the carbon $\pi - \pi$ bond energy, e is the electron charge.

III. FORCED STACK TECHNIQUE

Leakage current increases when threshold voltage decreases, this is a major component of leakage power and needs to be reduced. Stacking of transistor can reduce leakage power , a typical stacking technique can be seen in the fig 4[9]. Turning off the two transistors simultaneously suppresses the leakage power. The disadvantage of this technique is the increase in area but for us this will be a good option if we need some low power application.

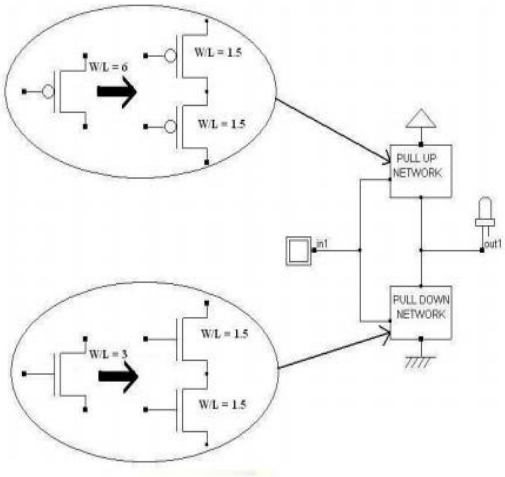

Fig. 3: Stack Technique

IV. CNTFET Based Low Power Clocked Pass Transistor Flip-Flop

Flip Flop is one bit storing element and a basic building block of memory devices.

But the circuit exhibits some leakage power dissipation and which can be reduced further. As the circuit is based on CNTFET so it is having low power but with the help of low power technique we will get better performance and more reduction in power.

There are several versions of Flip Flop generated by various research's, LCPTFF (Low Power Clocked Pass Transistor Flip-Flop)[10] is one of them. The schematic shown in Fig. 3 is a CNTFET based LCPTFF which uses the 6 transistors.

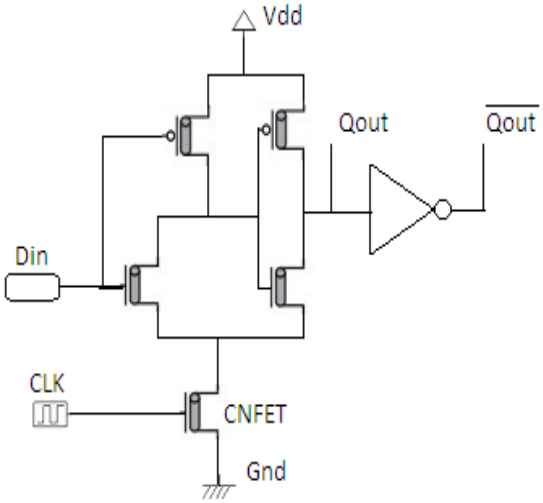

Fig.4: CNTFET Based LCPTFF (Low Power Clocked Pass Transistor Flip-Flop)

V. Proposed CNTFET Based Forced-Stack Low Power Clocked Pass Transistor Flip- Flop (CNTFET FS-LCPTFF)

We propose a CNTFET Based Forced Stack-LCPTFF (CNTFET-FS-LCPTFF) by applying a forced stack technique to the clock transistor as shown in Fig-5

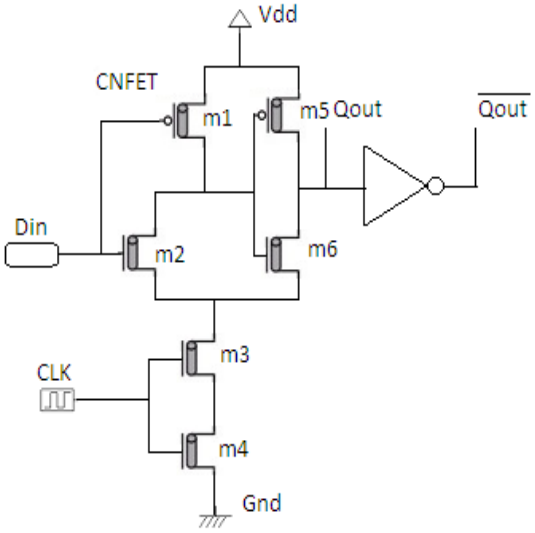

Fig.2: Proposed CNTFET Based Forced Stack-LCPTFF(CN-FS-LCPTFF)

The stacked transistor m3, m4 gets turnoff together when we apply low voltage, which reduces the subthreshold leakage power.

Now when clock is '1' and we apply Din = '1' then m2, m3,m4 are turned on and m1 turned off. So the output will be high as m5 will turned on.

When clock is '0' then both stacked CNTFET m3, m4 are turned off and the output will remain same until next clock pulse arrive. While switching off and on m3,m4 transistors together will reduces the leakage power.

Now when clock is '1' and Din is '0' then m1, m3, m4 transistors will tuned on which turned on m6 and ouput will be '0'.

Adding an extra transistor will increase the overall area of the chip but it will reduce the power which was our prime focus in the beginning of the research. The proposed design of D flip-flop is better in terms of power consumption.

VI. Simulation And Results

Our proposed CN-FS-LCPTFF and reference CN-LCPTFF are designed, simulated on HSPICE using Stanford CNTFET at 32nm technology. Results are carried out in the table 1,2 & 3.

Table 1,2 & 3 shows power consumption at 3 different temperature(25℃,50℃,75℃) with the variation of CNT diameter 1.01nm(m=13,n=0) and 1.487nm(m=19,n=0) shows that the technique we

applied on the low power clocked pass transistor flip flop reduce the power of the flip flip in ultra low power region by average power reduction on 12.7% for diameter of 1.01nm and 29% for diameter of 1.48 nm.

There are three charts shown in fig.6 , fig.7, fig.8 and we can observe that power consumption will increase while decreasing the CNTs diameter and viceversa. As we perfomed the simulation on three different temperature we can also state that the power consumption will increase wile increasing the temperature.

Power in nano Watt at three different power supply voltages with diameter variations on 25℃ temperature.

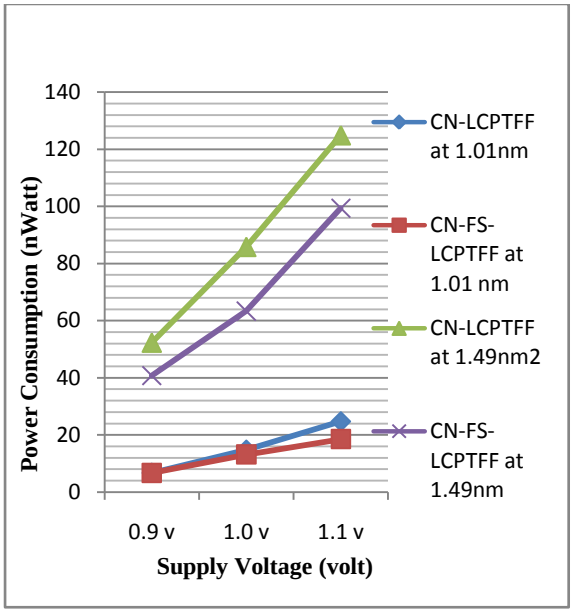

Fig. 3: Power Consumption vs Vdd (25 degree C)

Table 1 Comparison of Power Consumption between CN-LCPTFF and CN-FS-LCPTFF at 25°C

Design	Power Consumption In Nano Watt(nw)					
	CNT diameter 1.01nm			CNT diameter 1.487nm		
	Supply Voltage(v)			Supply Voltage(v)		
	0.9	1.0	1.1	0.9	1.0	1.1
CN-LCPTFF	6.71	17.79	24.7	52.25	85.8	124.9
CN-FS-LCPTFF	6.67	13.13	18.5	40.8	63.35	99.3
Power reduction(%)	0.59	11.2	25	23	26.6	20.1

Power in nano Watt at three different power supply voltages with diameter variations at 50 ℃ temperature.

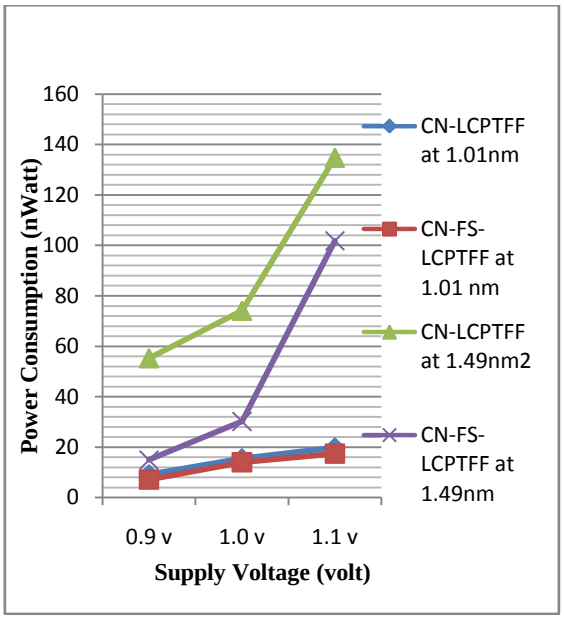

Fig. 4: Power Consumption vs Vdd (50 degree C)

Table 2 Comparison of Power Consumption between CN-LCPTFF and CN-FS-LCPTFF at 50°C

Design	Power Consumption In Nano Watt(nw)					
	CNT diameter 1.01nm			CNT diameter 1.487nm		
	Supply Voltage			Supply Voltage		
	0.9	1.0	1.1	0.9	1.0	1.1
CN-LCPTFF	9.15	15.55	19.88	55.3	74.15	134.8
CN-FS-LCPTFF	7.21	14	17.4	14.97	30.25	101.8
Power Reduction (%)	21	9.9	12.4	72	59.2	24

Power in nano Watt at three different power supply voltages with diameter variations at 75℃ temperature.

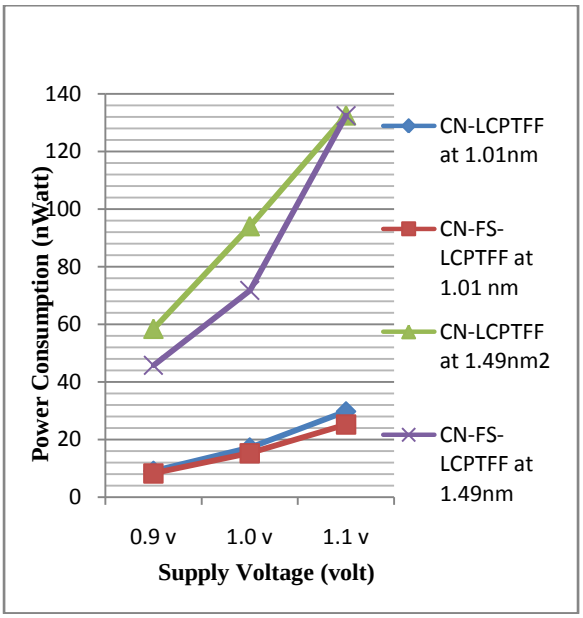

Fig. 8: Power Consumption vs Vdd (75 degree C)

Table 3 Comparison of Power Consumption between CN-LCPTFF and CN-FS-LCPTFF at 75°C

Design	Power Consumption In Nano Watt(nw)					
	CNT diameter 1.01nm			CNT diameter 1.487nm		
	Supply Voltage			Supply Voltage		
	0.9	1.0	1.1	0.9	1.0	1.1
CN-LCPTFF	9.17	17.2	29.8	58.5	94.15	132.6
CN-FS-LCPTFF	8.3	15.2	25.2	45.8	71.8	13
Power Reduction (%)	9.48	11	15	21.7	23.7	0.7

VII. CONCLUSION

In this paper the proposed CNTFET based D Flip-Flop reduces the subthreshold leakage current by applying the forced stack technique. While comparing the CN-FS-LCPTFF (proposed) and CN-LCPTFF (reference) at 100 Mhz, the proposed technique reduces the average power by 12 to 25%. The power reduction also depends on the diameter of the CNTs and temperature. The proposed CNTFET based Flip-Flop can be further used for making registers, counters, RAM and other memory devices.

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